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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,169	04/22/2004	Toshiharu Ueno	0879-0440PUS1	5771

2292 7590 08/08/2007
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EXAMINER	
RIAD, AMINE	
ART UNIT	**PAPER NUMBER**
2113	

NOTIFICATION DATE	DELIVERY MODE
08/08/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/829,169	UENO, TOSHIHARU	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-14 have been presented for examination.

Claims 1-14 have been rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4,9-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Krauch U.S. Patent 6,668,341.

In regard to claims 1 and 9,

Krauch discloses a method of recording and reproducing information in which a recording area of a recording medium is physically divided into small pages and is partitioned into separate physical blocks each having a plurality of the pages so that information is recorded and reproduced in units of the blocks to and from the recording medium, the method comprising the steps of: (Abstract) [Examiner considers the cell as a block and the cell latches as pages]

- upon recording of information in units of the blocks, recording a specific part of information, in a replicated manner, into each of the pages within the block;

(Column 3; lines 10-14 "there is implemented a third storing element in the storage element in the storage cell, which is depicted with reference sign 30, When a bit has to be written into the storage the respective value is concurrently written in all three elements 10,12,30 via one word lines associated with the write access circuit.")

- upon reproduction of the information recorded in the recording medium, reading the specific part of information and detecting an error in the read specific part of information; (Column 2; lines 60-62 "Writing the cell always writes both latches so that they hold the same data. A soft error can flip only one of the two latches. Then, a "XOR" block detects that the data is no longer identical. While the data is read out the check bit indicates that the data is corrupted")

- and when the error is detected in the specific part of information, correcting the error in the specific part of information based on a result of majority voting for a plurality of pieces of the specific part of information recorded in the replicated manner into the same block as where the error is detected.(Abstract; "Then, with the help of a small and simple error correction logic 32 in the cell from a majority vote can be seen which bit value is wrong in case of a soft error affecting one bit in the cell ")

In regard to claim 2

Krauch discloses the method of recording and reproducing information according to claim 1, wherein an error correction code is assigned to information in each of the

pages. (Column 3; lines 4-5 "Then, with the help of a small and simple error correction logic in the cell from a "majority vote" can be seen which bit value is wrong in case of a soft error ")

In regard to claim 3

Krauch disclose the method of recording and reproducing information according to claims 1, wherein the specific part of information is added with a parity bit that is one bit in size, and the error in the specific part of information is detected by parity checking.(Column 4; lines 57-58 "The check bit feature is functionally not nedded but optional for system error tracking")

In regard to claim 4

Krauch discloses the method of recording and reproducing information according to claims 2, wherein the specific part of information is added with a parity bit that is one bit in size, and the error in the specific part of information is detected by parity checking. (Figure 4; items cell0,cell1,cell2,check bit)

In regard to claim 10,

Krauch disclose the apparatus for recording and reproducing information according to claim 9, wherein the recording device calculates an error correction code for information in each of the pages recorded into the recording medium, and records a redundant part of the calculated error correction code together with the information of the page.

(Column 4; lines 41-44 "With reference to FIG. 4 the table is given from which the corrected data and the signal present on the check bit line 34 can be seen dependant ")

In regard to claim 11

Krauch discloses the apparatus for recording and reproducing information according to claims 9, wherein the recording device calculates a parity bit that is one bit in size for the specific part of information in each of the pages recorded into the recording medium, and adds the resultant parity bit to the specific part of information thereby to record the resultant information. (Column 4; lines 41-44 "With reference to FIG. 4 the table is given from which the corrected data and the signal present on the check **bit** line 34 can be seen dependant ")

In regard to claim 12

Krauch discloses the apparatus for recording and reproducing information according to claims 10, wherein the recording device calculates a parity bit that is one bit in size for the specific part of information in each of the pages recorded into the recording medium, and adds the resultant parity bit to the specific part of information thereby to record the resultant information. (Column 4; lines 41-44 "With reference to FIG. 4 the table is given from which the corrected data and the signal present on the check **bit** line 34 can be seen dependant ")

In regard to claim 13

Krauch discloses the apparatus for recording and reproducing information according to claim 11, wherein the error detection device detects the error in the specific part of information by applying parity checking to the specific part information in a head page within the block. (Figure 4; item=check bit)

In regard to claim 14

Krauch discloses the apparatus for recording and reproducing information according to claim 13, wherein the error correction device takes majority voting for each bit of the plurality of pieces of specific part of information and corrects the error bit by bit. (Column 4; lines 22-24 "the read access circuit which is the majority value of the three values stored in storing elements 10,12,30")

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5,6,7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krauch U.S. Patent 6,668,341 over Flaherty U.S. Patent 5,128,944.

Krauch discloses a method of recording and reproducing information.

Krauch does not disclose that the specific part of information is a logical address

Flaherty teaches that the specific part of information is a logical address. (Abstract; "each receiving the corresponding redundant data bits for one of the bits of an address byte")

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a logical address of Flaherty into the method of recording and reproducing information of Krauch. A person of ordinary skill in the art would have been motivated to apply a logical address of Flaherty because as Flaherty discloses "For either type of EPROM, write/erase operations are considerably more destructive more destructive of bit cell integrity than is a read operation...The most common technique for compensating for bit cell failures" Additionally, Krauch discloses "when a bit value changes due to such occurrences, so called soft errors have happened. In computer systems in which memory arrangements"

Response to Applicant's Argument

Applicant arguments filed on July 13, 2007 have been fully considered and are not persuasive.

In regard the argument which states "Applicant respectfully submits that the Krauch reference does not disclose the pages claimed in independent claims 1 and 9. As can be seen the pages relied on by Examiner are totally different in structure than the pages as claimed in independent in the present invention. In contrast, the pages as recited in claims are physical space capable of storing multi-bit data, information, logical address, and error correcting redundant information as shown"

Examiner repectfully disagrees. Examiner points out that claim language does not recite that pages are physical space capable of storing multi-bit data information, logical address and error correcting redundant information. As broadly recited, Krauch reads on claim 1 and 9. Further, Examiner will explain thoroughly how the latches of Krauch are the pages of present application. For this purpose, Examiner refers Applicant to Column 2 "Fig. 1- a schematic illustration of a storage cell implementation- which is drawn only schematically, but which shows clearly the write 14 and read circuitry 16 comprising m+1, and n+1 input, or output lines respectively with a respective write word line (WWL) or write bit line logic (WBL), or on the reading site- reading logic for word lines or bit lines (RWL, RBL). Such circuitry is required for writing or reading the bit value stored in the storing element 10 of the storage cell"

First, it is clear that element 10 is a transition between read circuit and write circuit 14 and 16. When Krauch disclosed that element 10 is a single bit latch, Krauch was giving an example an never was limited to a single bit only, as a proof for this is (Column 3; lines 35-36) "**Two storage elements 10, 12 which are adapted to store each one bit *e.g.***" Second Examiner points Applicant to (Column 4; lines 59-63) "It should be understood that storage cells as they are claimed in the appended claims can be incorporated into any-larger scale memory device". A larger scale memory would not work with a single bit latch, but instead with memory cells like registers or buffers. Examiner refers Applicant to the present application disclosures, and precisely to page 6 and paragraph one "According to the present invention, the same logical address is written, in a replicated manner, into each of all pages contained in one block" It is clear

that the only information replicated is the logical address, and nothing else as advanced by the Applicant in the above argument. This argument is not valid.

In regard the argument which states "If the multi-bit logical addresses of Flaherty were to be used to replace the single-bit storage elements of Krauch as suggested by the Examiner, it would totally contradict the main objective of Krauch invention" Examiner respectfully disagrees. Examiner states: since the assumption on which this argument is based on is false, the argument itself does not find solid support, and is very weak.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR
Amine Riad
Patent Examiner
7/31/2007